

**ABSTRACT OF THE DISCLOSURE**  
**COMPARE AND BRANCH MECHANISM**

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A data processing system is provided that includes an instruction decoder 20 responsive to a compare and branch instruction CHKA.X that performs a comparison between first and second values stored in first and second registers Rn, Rm  
10 respectively. A target branch address is determined from a pre-programmed stored value and a branch to a sub-routine is performed in dependence upon a result of the comparison.

[Figure 4]

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